Lecture 9

- region graph and the reachability problem
- model checking of timed automata

Automatic Verification of Timed Automata

Fact

Even very simple timed automata generate timed transition systems with infinitely (even uncountably) many reachable states.

Question

Is any automatic verification approach (like bisimilarity checking, model checking or reachability analysis) possible at all?

Answer

Yes, using region graph techniques.

Key idea: infinitely many clock valuations can be categorized into finitely many equivalence classes.

Intuition

Let $v, v' : C \to \mathbb{R}^{\geq 0}$ be clock valuations.
Let $\sim$ denote untimed bisimilarity of timed transition systems.

Our Aim

Define an equivalence relation $\equiv$ over clock valuations such that

1. $v \equiv v'$ implies $(\ell, v) \sim (\ell, v')$ for any location ℓ
2. $\equiv$ has only finitely many equivalence classes.

Preliminaries

Let $d \in \mathbb{R}^{\geq 0}$. Then

- let $\lfloor d \rfloor$ be the integer part of d, and
- let $\mathit{frac}(d)$ be the fractional part of d.

Any $d \in \mathbb{R}^{\geq 0}$ can be now written as $d = \lfloor d \rfloor + \mathit{frac}(d)$.

Example: $\lfloor 2.345 \rfloor = 2$ and $\mathit{frac}(2.345) = 0.345$.

Let A be a timed automaton and $x \in C$ be a clock. We define

$$c_x \in \mathbb{N}$$

as the largest constant with which the clock x is ever compared either in the guards or in the invariants present in A.

Clock (Region) Equivalence

Equivalence Relation on Clock Valuations

Clock valuations v and v' are equivalent ($v \equiv v'$) iff

1. for all $x \in C$ such that $v(x) \leq c_x$ or $v'(x) \leq c_x$ we have

$$\lfloor v(x) \rfloor = \lfloor v'(x) \rfloor$$

2. for all $x \in C$ such that $v(x) \leq c_x$ we have

$$frac(v(x)) = 0 \quad \text{iff} \quad frac(v'(x)) = 0$$

3. for all $x, y \in C$ such that $v(x) \leq c_x$ and $v(y) \leq c_y$ we have

$$frac(v(x)) \leq frac(v(y)) \quad \text{iff} \quad frac(v'(x)) \leq frac(v'(y))$$

Regions

Let v be a clock valuation. The $\equiv$-equivalence class represented by v is denoted by $[v]$ and defined by $[v] = \{v' \mid v' \equiv v\}$.

Definition of a Region

An $\equiv$-equivalence class $[v]$ represented by some clock valuation v is called a region.

Theorem

For every location ℓ and any two valuations v and v' from the same region ($v \equiv v'$) it holds that

$$(\ell, v) \sim (\ell, v')$$

where $\sim$ stands for untimed bisimilarity.

Symbolic States and Region Graph

state (ℓ, v) $\rightsquigarrow$ symbolic state $(\ell, [v])$

Note: $v \equiv v'$ implies that $(\ell, [v]) = (\ell, [v'])$.

Region Graph

The region graph of a timed automaton $A = (L, \ell_0, E, I)$ over a set of clocks C and a set of actions Act is an (untimed) labelled transition system $T_r(A) = (S, Act \cup \{\varepsilon\}, \{\overset{a}{\Longrightarrow} \mid a \in Act \cup \{\varepsilon\}\})$ where

- the states are the above symbolic states (thus S is finite)
- $(\ell, [v_1]) \overset{a}{\Longrightarrow} (\ell', [v_2])$ for $a \in Act$ iff
  $(\ell, v_1') \xrightarrow{a} (\ell', v_2')$ for some $v_1' \in [v_1]$, $v_2' \in [v_2]$
- $(\ell, [v_1]) \overset{\varepsilon}{\Longrightarrow} (\ell, [v_2])$ iff
  $(\ell, v_1') \xrightarrow{d} (\ell, v_2')$ for some $v_1' \in [v_1]$, $v_2' \in [v_2]$ and $d \in \mathbb{R}^{\geq 0}$

Application of Region Graphs to Reachability

We write $(\ell, v) \longrightarrow (\ell', v')$ whenever

- $(\ell, v) \xrightarrow{a} (\ell', v')$ for some label a, or
- $(\ell, v) \xrightarrow{d} (\ell', v')$ for some $d \in \mathbb{R}^{\geq 0}$.

Reachability Problem for Timed Automata

Instance (input): Automaton $A = (L, \ell_0, E, I)$ and a state (ℓ, v).

Question: Is it true that $(\ell_0, v_0) \longrightarrow^* (\ell, v')$ for some $v' \in [v]$?

(where $v_0(x) = 0$ for all $x \in C$)

Reduction of Timed Automata Reachability to Region Graphs

Reachability for timed automata is decidable because

$(\ell_0, v_0) \longrightarrow^* (\ell, v')$ for some $v' \in [v]$ in a timed automaton
if and only if $(\ell_0, [v_0]) \Longrightarrow^* (\ell, [v])$ in its (finite) region graph.

Applicability of Region Graphs

Pros

Region graphs provide a natural abstraction which enables to prove decidability of e.g.

- reachability
- timed and untimed bisimilarity
- untimed language equivalence and language emptiness.

Cons

Region graphs have too large state spaces. State explosion is exponential in

- the number of clocks
- the maximal constants appearing in the guards.

Zones and Zone Graphs

Zones provide a more efficient representation of symbolic state spaces. A number of regions can be described by one zone.

Zone

A zone is described by an extended clock constraint $g \in \mathcal{B}^+(C)$.

$$g \;::=\; x \sim n \;\mid\; x - y \sim n \;\mid\; g_1 \wedge g_2$$

(also the so called diagonal constraints $x - y \sim n$ are now allowed)

Region Graphs

symbolic state: $(\ell, [v])$
where v is a clock valuation

Zone Graphs

symbolic state: $(\ell, [g])$
where g is an extended clock constraint

A zone is usually represented (and stored in the memory) as
DBM (Difference Bound Matrix).

Logic for Timed Automata in UPPAAL

Let ϕ and ψ be local properties (check-able locally in a given state).

Example: (H.busy $\wedge$ W.rest $\wedge$ $20 \leq z \leq 30$)

UPPAAL can check the following formulae (subset of TCTL)

- A[]ϕ — invariantly ϕ
- E$\langle\rangle\phi$ — possibly ϕ
- A$\langle\rangle\phi$ — always eventually ϕ
- E[]ϕ — potentially always ϕ
- ϕ –> ψ — ϕ always leads to ψ (same as A[]($\phi \implies$ A$\langle\rangle\psi$))

Legend:

- A and E are so called path quantifiers, and
- [] and $\langle\rangle$ quantify over states of a selected path.